REMARKS

This Amendment is being filed in response to the Final Office Action mailed August 4, 2009, which has been reviewed and carefully considered. Reconsideration and allowance of the present application in view of the amendments made above and the remarks to follow are respectfully requested.

Claims 1-2 and 4-25 are pending in this application, where claims 24-25 had been previously added added. Claims 1, 12, 18-19 and 21 are independent.

By means of the present amendment, the current Abstract has been deleted and substituted with the enclosed New Abstract which better conforms to U.S. practice. Further, the specification has been amended for better conformance with the drawings.

In the Office Action, claims 12-17 are rejected under 35 U.S.C. §112, second paragraph. This rejection is respectfully traversed. However, without agreeing with the position forwarded in the Office Action and in the interest of advancing prosecution, claims 12-13 and 16-17 have been amended. It is respectfully

submitted that this rejection has been overcome. Accordingly, withdrawal of this rejection is respectfully requested.

In the Office Action, claims 1, 4-6, 8, 11-14, 16, 18 and 22-23 are rejected under 35 U.S.C. §103(a) over U.S. Patent No. 5,752,035 (Trimberger). Further, claims 2, 9-10, 17, 19-20 and 24-25 are rejected under 35 U.S.C. §103(a) over Trimberger in view of U.S. Patent No. 5,696,956 (Razdan). Claims 7 and 21 are rejected under 35 U.S.C. §103(a) over Trimberger in view of U.S. Patent No. 6,327,704 (Mattson). In addition, claim 15 is rejected under 35 U.S.C. §103(a) over Trimberger in view of Official Notice. It is respectfully submitted that claims 1-2 and 4-25 are patentable over Trimberger, Razdan, Mattson and Official Notice for at least the following reasons.

Trimberger is directed to a method for compiling and executing programs for a reprogrammable instruction set accelerator (RISA). A computer program is translated into executable code using RISA instructions.

As shown in FIG 1, and described on column 7, lines 30-65, a data processing system includes a host CPU 10 with internal buses

22, 23. A fixed **internal** execution unit 24 and an **internal** RISA 21 are coupled to the internal buses 22 and 23. "The RISA 21 comprises a field programmable gate array 30, which includes a configuration store 31." (Trimberger, column 7, lines 55-56)

Techniques for deciding which instructions to configure into the RISA are provided. As recited on column 15, lines 19-23:

> most commonly used sequences, which may be bounded by size to manage development of the RISAs, are collected into separate groups. Each group is optimized to form a single RISA instruction that performs the whole task. (Emphasis added)

That is, a maximum size is set for the most commonly used sequences, which are "bounded by size to manage development of the RISAs." (Column 15, lines 20-21; emphasis added) Each group of the most commonly used sequences forms "a single RISA instruction that performs the whole task." (Column 15, lines 22-23; emphasis added)

Further, column 15, lines 41-44 recites that:

> **least used** RISA instructions are **converted back into fixed instructions**, or to a combination of fixed instructions and simpler RISA instructions, until the used RISA instructions fit within the available configurable resources. (Emphasis added)

It is respectfully submitted that Trimberger does not teach or suggest the combinations of elements as recited in the independent claims. Furthermore, each independent claim includes at least one claim element not found anywhere in Trimberger. For example the method of claim 1 recites (illustrative emphasis provided):

> detecting a **number** of **external** processing units connected to ports of the apparatus, the external processing units being **external** to the apparatus;
> providing an **index information indicating the repetition frequency** of said repeated sub-sequence, wherein said index information comprises an **integer** number set in **proportion with a ranking** of said repetition rate of said repeated sub-sequence compared to the repetition rate of other detected repeated sub-sequences; and
> determining an allocation between the **external processing units** and said repeated sub-sequence based on said index information.

Detecting the **number** of **external** processing units and determining an allocation between the **external** processing units and the repeated sub-sequence, as recited in independent claim 1, is nowhere disclosed or suggested in Trimberger. Rather, Trimberger a fixed **internal** execution unit 24 and an **internal** RISA 21 coupled to the internal buses 22, 23, as shown in FIG 1, and described on column 7, lines 30-65.

In addition, Trimberger does not even disclose or suggest an index information indicating the repetition frequency of a repeated sub-sequence, let alone disclosing or suggesting that the index information comprises an integer number set in proportion with a ranking of the repetition rate.

Assuming, arguendo, that Trimberger discloses or suggests ranking of most and least commonly used sequences (which it does not), any such ranking is used to **synthesizes** "a new programmed **instruction** for commonly used sequences." (Trimberger, column 15, lines 2-3; emphasis added) Further, the "least used RISA instructions are **converted back** into fixed instructions." (Trimberger, column 15, lines 41-42; emphasis added) That is, any ranking in Trimberger is used to synthesizes a new RISA instructions, or convert back RISA instructions into fixed instructions. There is simply no disclosure or suggestion in Trimberger to provide an index information indicating the repetition frequency of the repeated sub-sequence, where the index information comprises an integer number set in proportion with a ranking of the repetition rate of the repeated sub-sequence

compared to the repetition rate of other detected repeated sub-sequences; and determining an allocation between the external processing units and the repeated sub-sequence based on the index information, as recited in independent claim 1.

The apparatus of independent claim 12 and the compiler of independent claim 18 include similar language to that emphasized above for independent claim 1. Applicant respectfully submits that independent claims 12 and 18 also are separately patentable for at least similar reasons.

Further, in rejecting independent claim 19, on page 13, last paragraph of the Office Action, the Examiner correctly noted that Trimberger does not disclose or suggest "add to said repeated sub-sequence an instruction specifying said index information," as recited in independent claim 19. Razdan is cited in an attempt to remedy the deficiencies in Trimberger.

Razdan is directed to a dynamically programmable reduced instruction set computer. As recited on column 4, lines 39-41, "an additional opcode, the EXPFU Opcode is included in the instruction set. The purpose of the EXPFU Opcode is to identify the instruction

as one associated with the PFU." Column 4, lines 51-57 further recite:

> The LPnum field is an 11-bit field to **define a particular logical function** to be performed by the PFU unit 24. The LPnum field is only of interest when the opcode field is encoded to indicate an EXPFU instruction. The LPnum field is basically an identifier corresponding to an available programming configuration for the PFU for a given application.

On page 14, lines 9-11 of the Office Action, it is alleged that the LPnum field is index information representing a frequency of execution of replaced sub-sequence of instruction. Applicant respectfully disagrees and submits that the "LPnum field is an 11-bit field to define a particular logical function," as specifically recited on column 4, lines 51-52 of Razdan.

It is respectfully submitted that Trimberger, Razdan, and combination thereof, do not teach or suggest "index information indicating the repetition frequency of said repeated sub-sequence," and adding "to said repeated sub-sequence an instruction specifying said index information," as recited in independent claim 19.

Similar to the compiler of independent claim 19, the compiler of independent claim 21 comprises combinations of claim elements

not found in Trimberger and Razdan. In particular, Trimberger, Mattson, and combination thereof, do not teach or suggest to "provide an index information indicating the repetition frequency of said repeated sub-sequence, wherein said compiler is arranged to add to said output sequence an instruction for indicating that said repeated sub-sequence is not used anymore," as recited in independent claim 21.

Mattson and Official Notice are cited to allegedly show other features and do not remedy the deficiencies in Trimberger and Razdan.

Based on the foregoing, it is respectfully submitted that independent claims 1, 12, 18-19 and 21 are allowable over Trimberger, and notice to this effect is earnestly solicited. Claims 2, 4-11, 13-17, 20 and 22-25 respectively depend from one of claims 1, 12, 18-19 and 21 and accordingly are allowable for at least this reason as well as for the separately patentable elements contained in each of said claims. Accordingly, separate consideration of each of the dependent claims is respectfully requested.

For example, claim 4 recites that "said allocation is determined by comparing said integer number with the number of available processing resources." (Illustrative emphasis provided) These features are nowhere disclosed or suggested in Trimberger. Rather, column 15, lines 39-44 of Trimberger, cited on page 10 of the Office Action in rejecting claim 4, merely recites that the "least used RISA instructions are **converted back** into fixed instructions, or to a combination of fixed instructions and simpler RISA instructions, **until** the used RISA instructions fit within the available configurable resources." (Emphasis added)

Even assuming, arguendo, that Trimberger is concerned with determining allocation between the external processing units and the repeated sub-sequence based on the index information that indicates the repetition frequency of the repeated sub-sequence, there are innumerable ways to determine such an allocation where, assuming, arguendo, one way is to convert back RISA instructions into fixed instructions, as disclosed in Trimberger. Determining allocation by converting back instructions does not disclose or suggest determining allocation "by comparing said integer number

with the number of the external processing units," as recited in claim 4, where the integer number is set in proportion with a ranking of the repetition rate.

In addition, the recitation on column 15, lines 19-23 of Trimberger, cited in rejection claim 6 on page 11 of the Office Action, that the "most commonly used sequences, which may be bounded by size to manage development of the RISAs, are collected into separate groups," merely discloses that the most commonly used sequences are collected in a groups that have a maximum size or are "bounded by size to manage development of the RISAs." (Emphasis added) The disclosure that a group has a maximum size does not disclose or suggest that "said index information comprises an information indicating the **number** of instructions in said repeated sub-sequence," as recited in claim 6. (Illustrative emphasis provided)

Further, in rejecting claim 13, on page 12 of the Office Action, FIG 1 item 22 of Trimberger is cited. It is respectfully submitted that item 22 is an **internal** bus, and does not disclose or suggest "**ports** for connecting at least one **external** processing unit

to which said repeated sub-sequence can be allocated," as recited in claim 13. (Illustrative emphasis provided)

In addition, in rejecting claim 9, on page 15 of the Office Action, column 7, line 66 to column 8, line 3 of Trimberger, is cited. It is respectfully submitted that column 7, line 66 to column 8, line 3 of Trimberger specifically recite:

> A configuration store 31 is coupled with the field programmable gate array 30. The configuration store 31 may accessible through a dedicated port generally 35, or by means of the internal buses 22 and 23 for dynamically reprogramming in a field programmable gate array 30.

That is, a memory is provided which is accessible through a dedicated port or an internal bus for dynamically reprogramming in a field programmable gate array. Such a disclosure has nothing to do, and does not disclose or suggest, "activating an external processing unit of the external processing units when said instruction containing said index information indicates that the corresponding repeated sub-sequence has already been allocated to said external processing unit," as recited in claim 9. (Illustrative emphasis provided)

Further, "additional instruction is added so as to precede

said repeated sub-sequence," as recited in claim 20, is nowhere disclosed or suggested in Trimberger. Rather, column 13, lines 30-33, cited on page 15 of the Office Action, specifically disclose that a "programmed instruction is then executed upon detection of an access to the start of the sequence in the cache, or the program can be re-compiled to include the new programmed instruction." Executing an instruction upon detection of access to the start of a sequence, does not disclose or suggest adding an additional instruction, specifying the index information, so as to precede the repeated sub-sequence, as recited in claim 20.

In addition, Applicant denies any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicant reserves the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded. And in particular, no Official Notices are conceded.

In view of the above, it is respectfully submitted that the present application is in condition for allowance, and a Notice of Allowance is earnestly solicited.

Respectfully submitted,

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